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What Is Claimed Is:

	<u> </u>
1 ,	An apparatus for compressing video data, comprising: a video input port, for receiving video data for a current video frame;
Sele	a video input port, for receiving video data for a current video frame;
3	a video input buffer coupled to the video input port, for storing video data
4	from the video input port;
5	a previous frame buffer, for storing at least a portion of a previous video
6	frame;
7	an operation unit coupled to the video input buffer and the previous frame
8	buffer, for performing an operation between data from the video input buffer and
9	data from the previous frame buffer; and
10	a result buffer coupled to the operation unit, for storing the result of an
11	operation from the operation unit.

- The apparatus of claim 1, including a memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a memory that stores video data from the video input fort and result data from the result buffer.
- The apparatus of claim 2, including a memory coupled to the 3. 1 memory port for storing the video data from the video input port and result data 2 from the result buffer, wherein the vide data is stored to in a current frame area 3 in the memory and the result data is stored in a difference frame area in the 4 5 memory.
- The apparatus of claim 3, wherein the memory stores a current 4. 1 video frame and a previous video frame in the same location in the memory, 2 allowing the current vided frame to be written over the previous video frame. 3

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- The apparatus of claim 3, wherein the memory also stores 5. instructions and data for a central processing unit of a computer system.
- The apparatus of claim 1, wherein the operation unit performs an 6. 1 exclusive-OR operation between data from the video input buffer and data from 2 the previous frame buffer. 3
- The apparatus of claim 1, wherein: 7. 1 the video input buffer stores a block of data from the video input port; 2 the previous frame buffer stores a block of data from the previous video 3 4 frame; the result buffer stores/a block of data from the operation unit; and 5 the operation unit performs an operation between a block of data from the 6 video input port and a block of data from the previous frame buffer.
- The apparatus of claim 1, wherein the apparatus resides inside of a 8. 1 core logic chip for a computer system. 2
- The apparatus of claim 1, wherein the apparatus comprises part of 9. 1 a video conferencing system. 2
- The apparatus of claim 1/including additional resources within the 10. 1 apparatus, for compressing the video data from the video input port. 2
- The apparatus of claim 1, including a color space conversion 11. 1 circuit coupled between the video input port and the video input buffer. 2

13

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1	12. The apparatus of claim 1, wherein the video input buffer is a
2	register that stores less than one video frame.
1.	An apparatus for compressing video data, comprising:
Sant	a video input port, for receiving video data for a current video frame;
عليه	a video input buffer coupled to the video input port, for storing video data
4	from the video input port;
5	a previous frame buffer, for storing at least a portion of a previous video
6	frame;
7	an exclusive-OR unit coupled to the video input buffer and the previous
8	frame buffer, for performing an exclusive-OR operation between data from the
9	video input buffer and data from the previous frame buffer;
10	a result buffer coupled to the operation unit, for storing the result of an
11	operation from the operation unit;
12	a memory port coupled to the previous frame buffer and the result buffer,
13	for transferring data to and from a memory that stores video data from the video
14	input port and result data from the result buffer; and
15	a memory coupled to the memory port for storing the video data from the
16	video input port and result data from the result buffer, wherein the video data is
17	stored to in a current frame in the memory and the result data is stored in a
18	difference frame in the memory.
/ 1 /	14. The apparatus of claim 13, wherein the memory stores a current
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video frame and a previous video frame in the same location, allowing the current

video frame to be written over the previous video frame.

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1	15. The apparatus of claim 13, wherein the memory stores instructions
2	and data for a central processing unit of a computer system.
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1	16. The apparatus of claim 13, wherein:
2	the video input buffer stores a block of data from the video input port;
3	the previous frame buffer stores a block of data from the previous video
4	frame;
5	the result buffer stores a block of data from the operation unit; and
6	the explusive-OR unit performs an exclusive-OR operation between a
7	block of data from the video input port and a block of data from the previous
	frame buffer.
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1	17. The apparatus of claim 13, wherein the apparatus resides inside of
2	a core logic chip for a computer system.
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1	18. The apparatus of claim 13, wherein the apparatus comprises part of
2	a video conferencing system.
1	19. The apparatus of claim 13, including a color space conversion
2	circuit coupled between the video input port and the video input buffer.
	,
,1	$\lambda^3 > 20$. A computer system including resources for compressing video,
l.b	comprising:
3	a central processing unit within the computer system;
4	a video input port, for receiving video data for a current video frame;
4	the storing video data
	from the video input port;
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	1	a previous frame buffer, for storing at least a portion of a previous video
123 0	2	frame:
1	3	an operation unit coupled to the video input buffer and the previous frame
Coul	4	buffer, for performing an operation between data from the video input buffer and
	5	data from the previous frame buffer; and
	6	a result buffer coupled to the operation unit, for storing the result of an
	7	operation from the operation unit.